UTRON

UT621024

Rev. 1.4

128K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time : 35/55/70ns (max.)
- Low power consumption :
  Operating : 60/40 mA (typical)
  Standby : 10μA (typical) L-version
  1μA (typical) LL-version
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 32-pin 600 mil PDIP
  32-pin 450 mil SOP
  32-pin 8x20mm TSOP-1
  32-pin 8x13.4mm STSOP

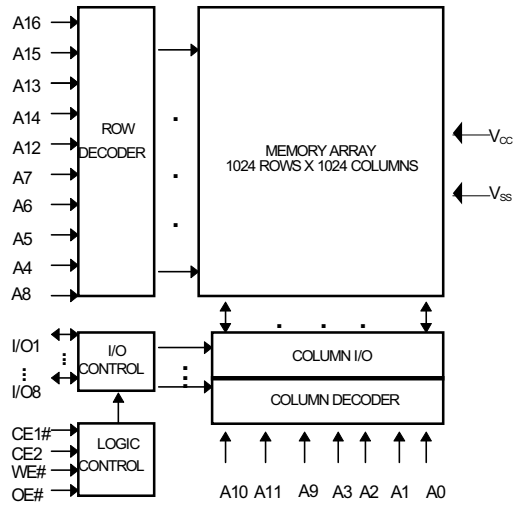
GENERAL DESCRIPTION

The UT621024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

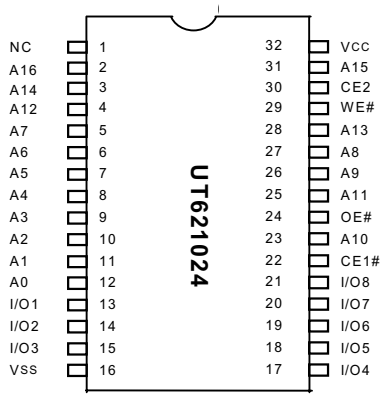
The UT621024 is designed for low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT621024 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

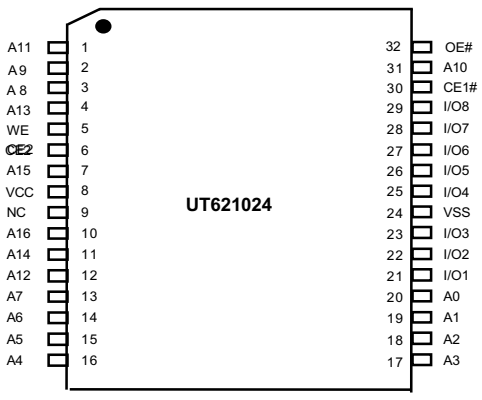
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PDIP/SOP



TSOP-1/STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#, CE2	Chip Enable 1,2 Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V± 10%, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ CE1# =V_{IH} or CE2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL}		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH} = - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
Average Operating Power Supply Courrent	I_{CC}	Min.Cycle, 100% Duty, CE1# =V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0mA	-35	-	60	100	mA
			-70	-	40	70	mA
	I_{CC1}	Cycle time = 1μs, 100% Duty, CE1#≦0.2V,CE2≧V_{CC}-0.2V, $I_{I/O}$ = 0mA		-	-	10	mA
Standby Power Supply Current	I_{SB}	CE1# =V_{IH} or CE2 = V_{IL}		-	-	3	mA
	I_{SB1}	CE1#≧V_{CC}-0.2V or CE2≦0.2V	- L	-	10	300	μA
						100*	
			- LL	-	1	50	μA
						15*	

*Those parameters are for reference only under 50℃

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=100pF, I_{OH}/I_{OL}=-1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V± 10% , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT621024-35		UT621024-55		UT621024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	35	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ1}*, t_{CLZ2}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}*, t_{CHZ2}*	-	25	-	30	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	25	-	30	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns

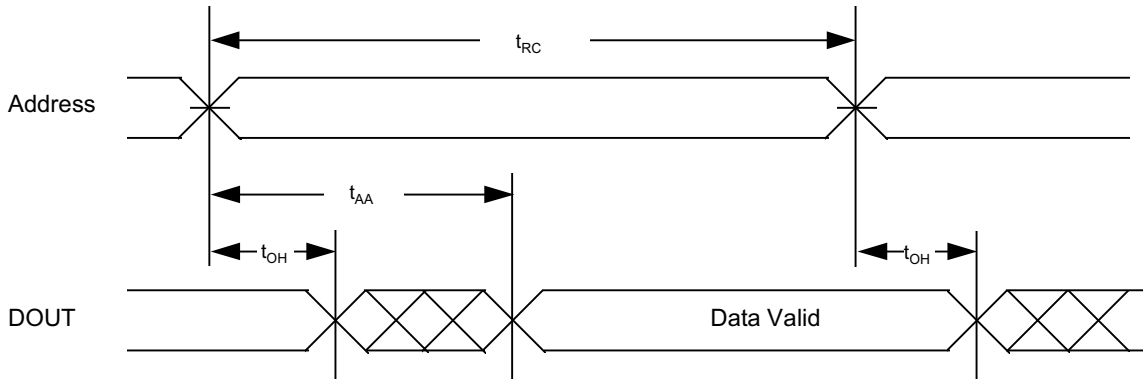
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT621024-35		UT621024-55		UT621024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	30	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	40	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

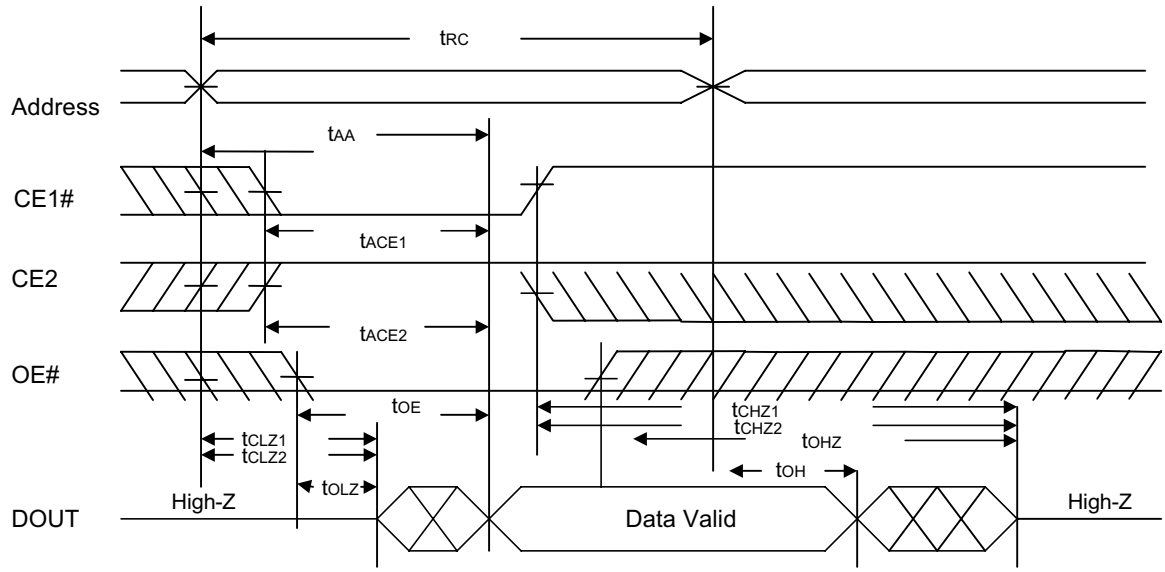
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

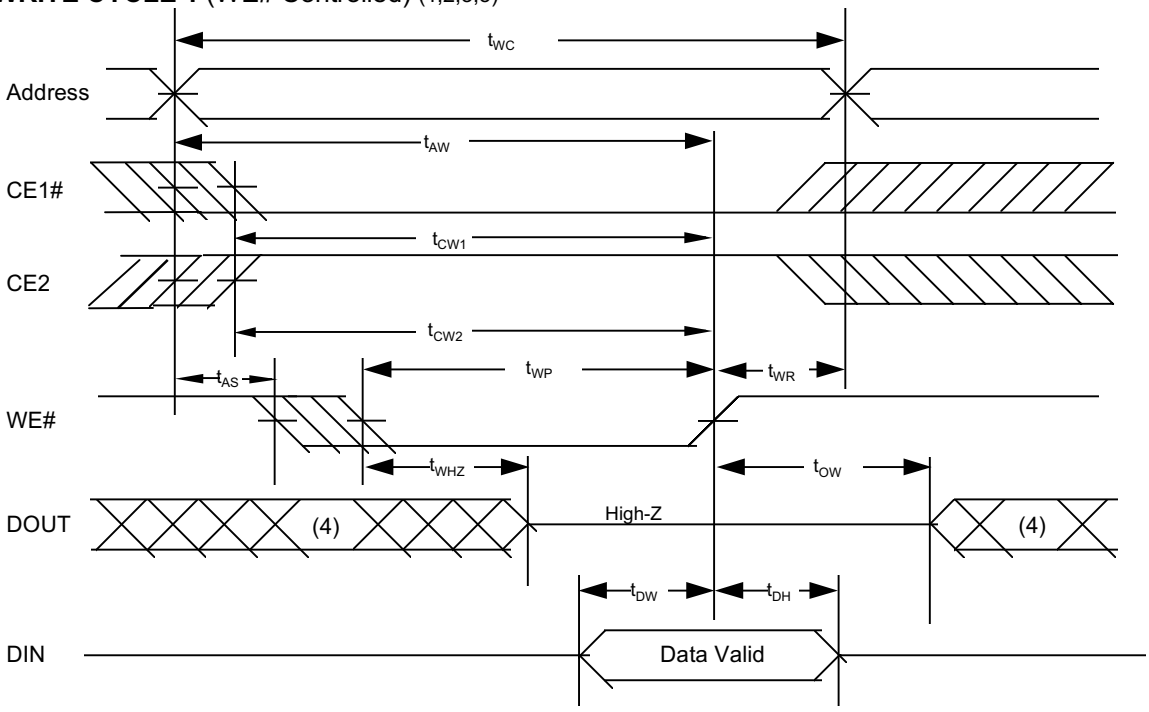


READ CYCLE 2 (CE1#, CE2 and OE# Controlled) (1,3,5,6)

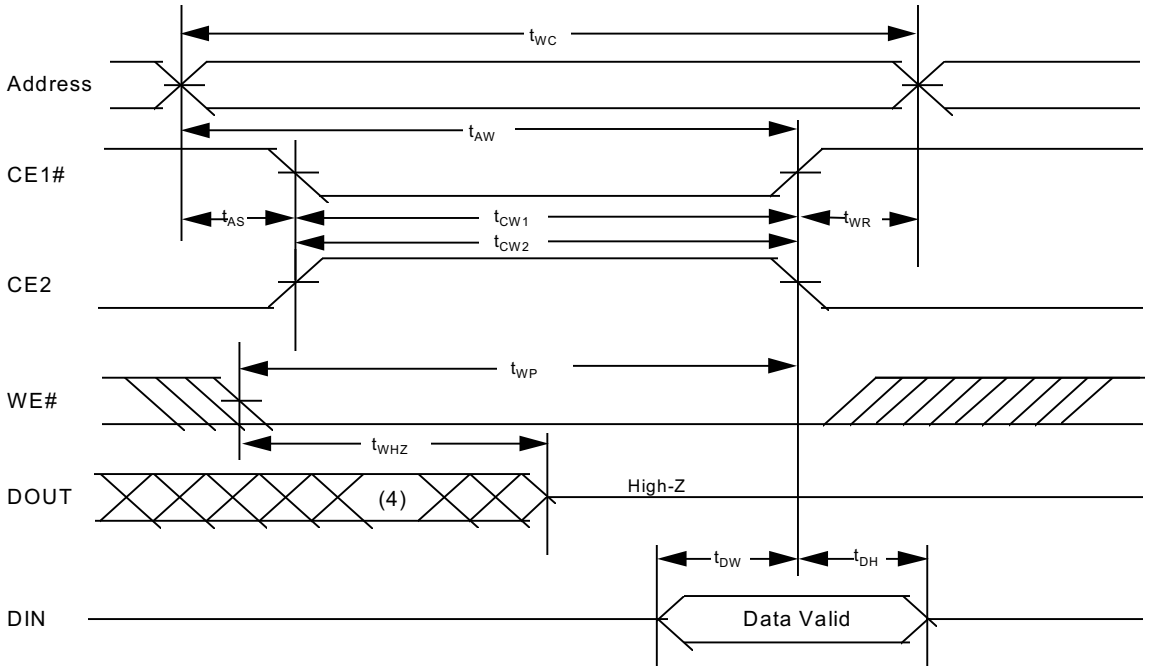


Notes :
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE1#=V_{IL} and CE2=V_{IH}.
3. Address must be valid prior to or coincident with CE1# and CE2 transition; otherwise t_{AA} is the limiting parameter.
4. OE# is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



WRITE CYCLE 2 (CE1# and CE2 Controlled) (1,2,5)



Notes :
1. WE# or CE1# must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low CE1#, a high CE2 and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the CE1# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.

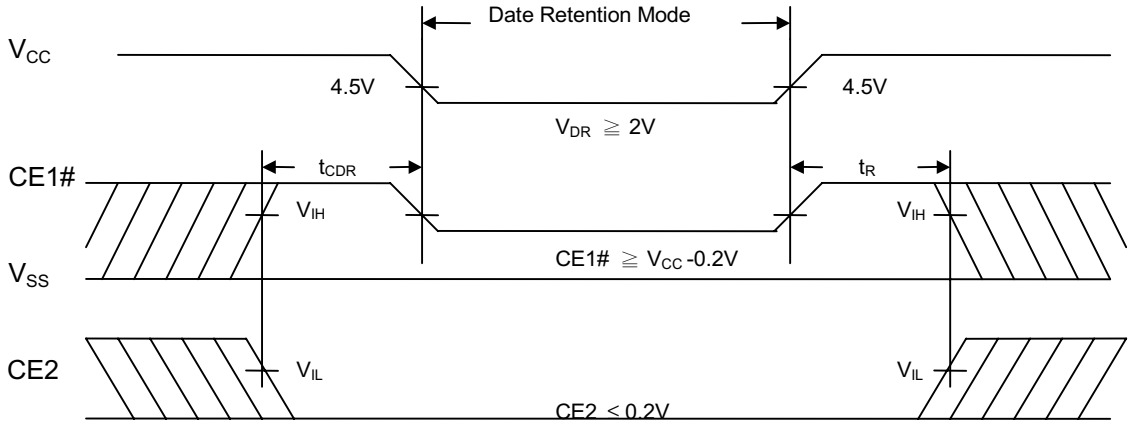
DATA RETENTION CHARACTERISTICS (T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	CE1# ≧ V_{CC}-0.2V or CE2 ≤ 0.2V		2.0	-	-	V
Data Retention Current	I_{DR}	Vcc=3V	- L	-	5	100 / 50*	µA
		CE1# ≧ V_{CC}-0.2V or CE2 ≤ 0.2V	- LL	-	0.5	20 / 10*	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC}*	-	-	ns

t_{RC}* = Read Cycle Time

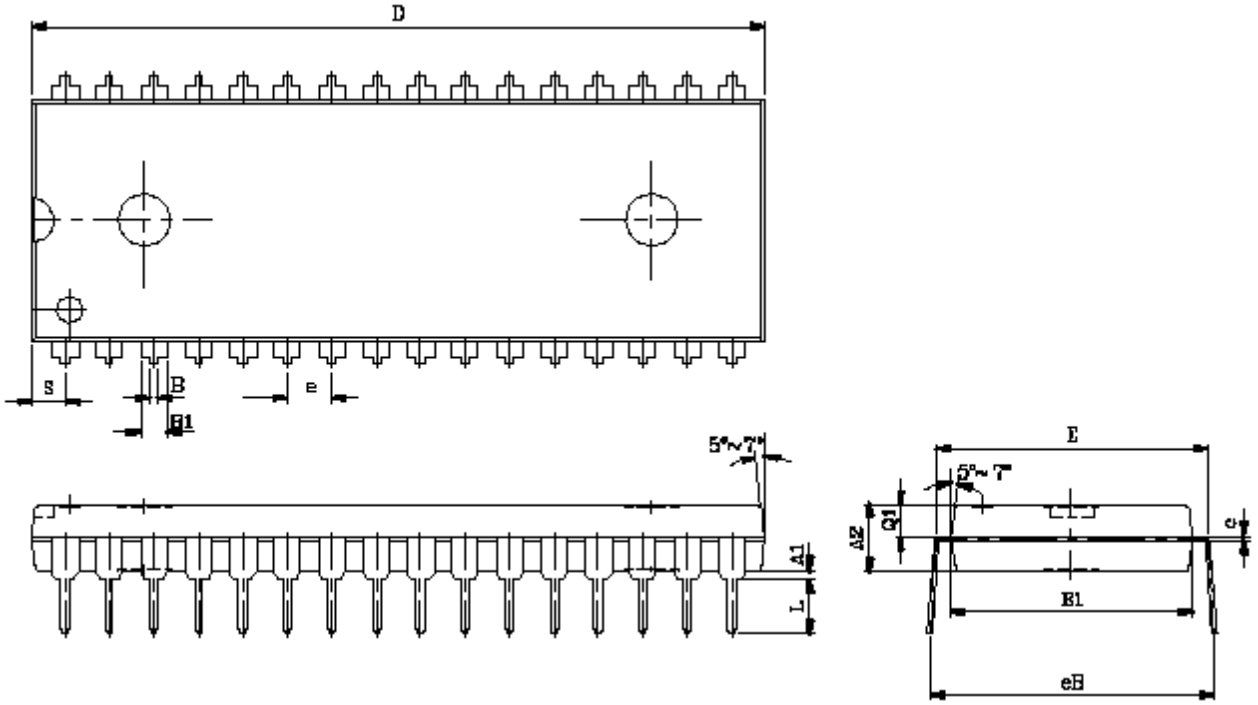
*Those parameters are for reference only under 50℃

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

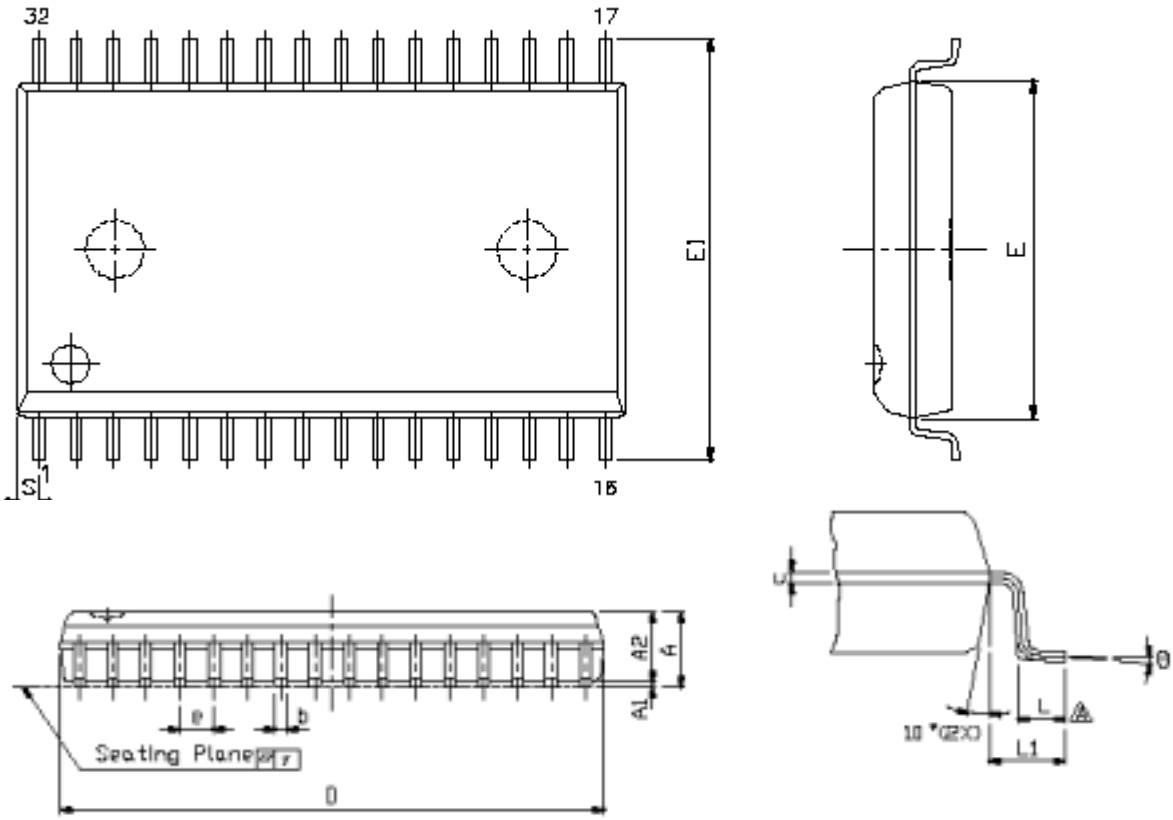
32PIN 600 milPDIP PACKAGE OUTLINE DIMENSION



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150 ± 0.005	3.810 ± 0.127
B	0.018 ± 0.005	0.457 ± 0.127
△ B1	0.050 ± 0.005	1.270 ± 0.127
c	0.010± 0.004	0.254± 0.102
D	1.650 ± 0.005	41.910 ± 0.127
△ E	0.600 ± 0.010	15.240 ± 0.254
E1	0.544 ± 0.004	13.818 ± 0.102
e	0.100(TYP)	2.540(TYP)
eB	0.640 ± 0.020	16.256 ± 0.508
L	0.130 ± 0.010	3.302 ± 0.254
S	0.075 ± 0.010	1.905± 0.254
Q1	0.070± 0.005	1.778± 0.127

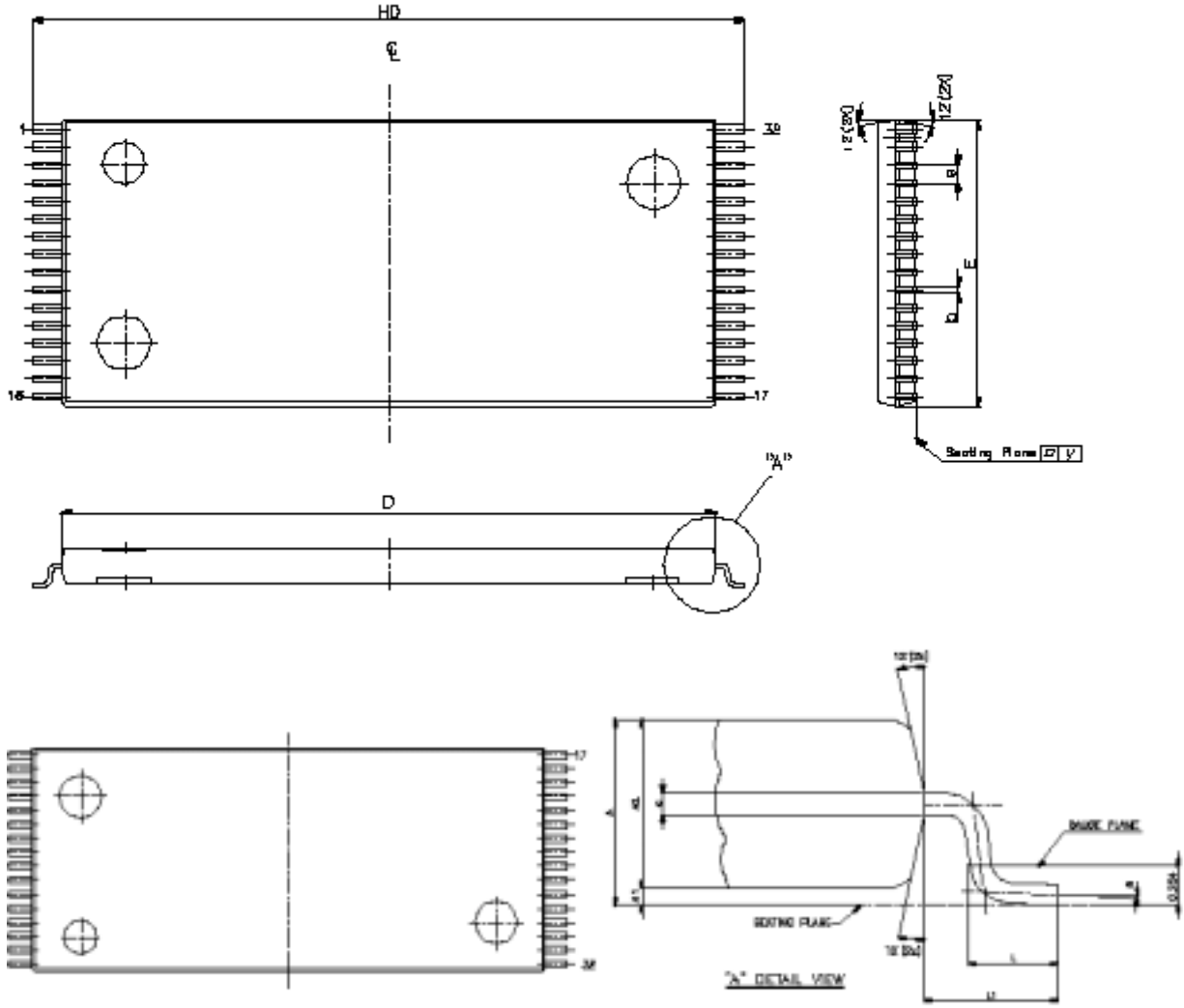
Note:
1. D/E1/S DIMENSION DO NOT INCLUDE MOLD FLASH.

32pin 450mil SOP PACKAGE OUTLINE DIMENSION



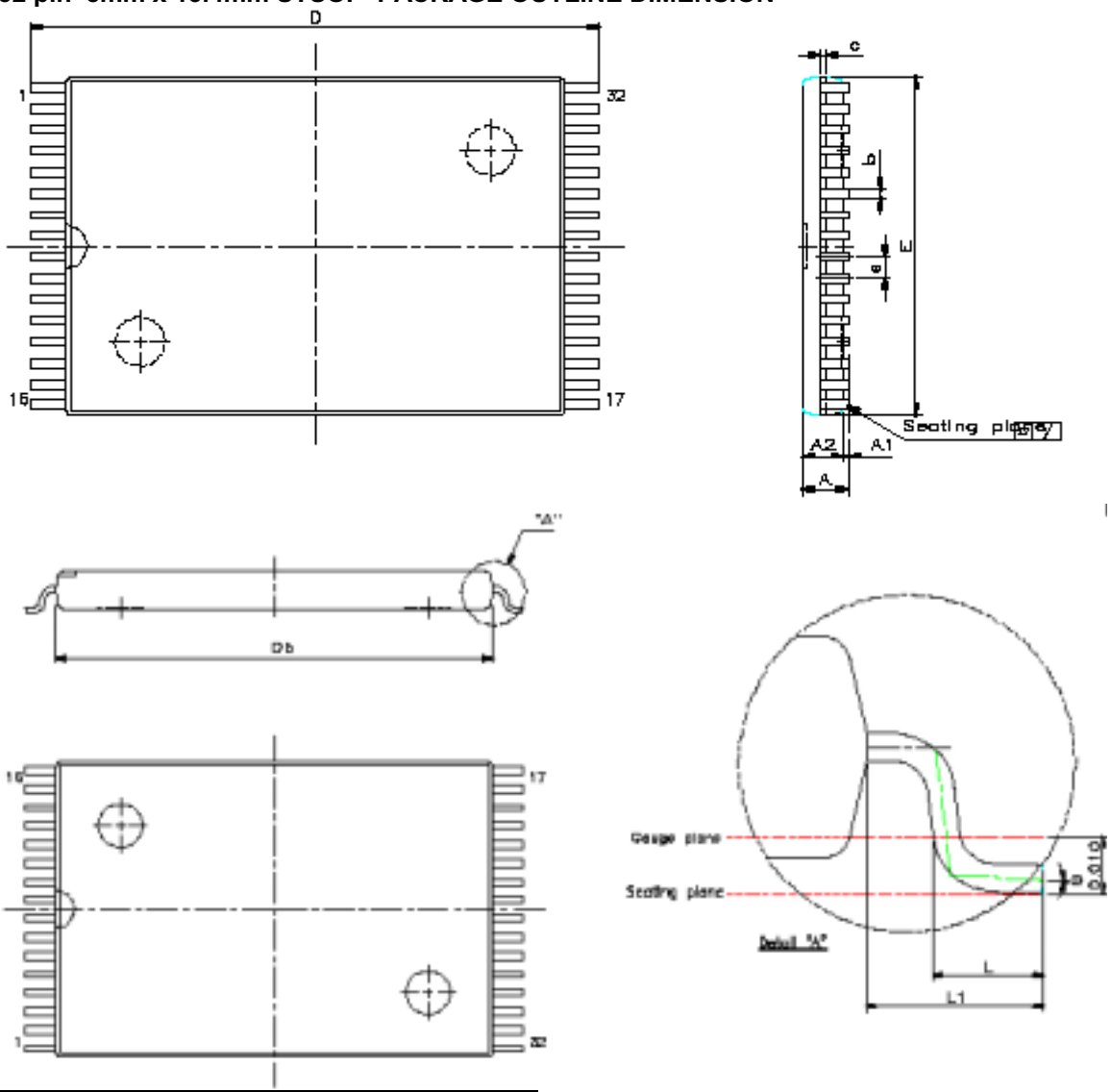
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.111(MAX)	2.82(MAX)
b	0.015(MIN) 0.020(MAX)	0.38(MIN) 0.50(MAX)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
△A E	0.445 ± 0.005	11.303 ± 0.127
E1	0.555 ± 0.005	14.097 ± 0.127
e	0.050(TYP)	1.270(TYP)
△A L	0.0347 ± 0.008	0.881 ± 0.203
L1	0.055 ± 0.008	1.397 ± 0.203
S	0.026(MAX)	0.660 (MAX)
△C y	0.004(MAX)	0.101(MAX)
θ	0^o -10^o	0^o -10^o

32pin TSOP-I PACKAGE OUTLINE DIMENSION



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
△C A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
△E △C b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ± 0.004	18.40 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ± 0.008	20.00 ± 0.20
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.08 ± 0.10
△H y	0.003 (MAX)	0.076 (MAX)
△B θ	0°～5°	0°～5°

32 pin 8mm x 13.4mm STSOP PACKAGE OUTLINE DIMENSION



Unit / Symbol	mm(ref)	inch(base)
A	1.20(Max.)	0.047(Max).
A1	0.10±0.05	0.004±0.002
A2	1.00±0.05	0.039±0.002
b	020(typ.)	0.006(typ.)
c	0.15(typ.)	0.006(typ.)
D	13.40±0.20	0.526±0.006
Db	11.80±0.10	0.465±0.004
E	8.000±0.10	0.315±0.004
e	0.50(typ.)	0.020(typ.)
L	0.50±0.10	0.020±0.004
L1	0.80±0.10	0.0315±0.004
y	0.08(Max.)	0.003(Max.)
e	0°~5°	0°~5°

Note：
E dinmension is not including end flash.
The total of both sides' end flash Is not above 0.3mm.

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA)	PACKAGE
UT621024PC-35L	35	300	32PIN PDIP
UT621024PC-35LL	35	50	32PIN PDIP
UT621024SC-35L	35	300	32PIN SOP
UT621024SC-35LL	35	50	32PIN SOP
UT621024LC-35L	35	300	32PIN TSOP-I
UT621024LC-35LL	35	50	32PIN TSOP-I
UT621024LS-35L	35	300	32PIN STSOP
UT621024LS-35LL	35	50	32PIN STSOP
UT621024PC-55L	55	300	32PIN PDIP
UT621024PC-55LL	55	50	32PIN PDIP
UT621024SC-55L	55	300	32PIN SOP
UT621024SC-55LL	55	50	32PIN SOP
UT621024LC-55L	55	300	32PIN TSOP-I
UT621024LC-55LL	55	50	32PIN TSOP-I
UT621024LS-55L	55	300	32PIN STSOP
UT621024LS-55LL	55	50	32PIN STSOP
UT621024PC-70L	70	300	32PIN PDIP
UT621024PC-70LL	70	50	32PIN PDIP
UT621024SC-70L	70	300	32PIN SOP
UT621024SC-70LL	70	50	32PIN SOP
UT621024LC-70L	70	300	32PIN TSOP-I
UT621024LC-70LL	70	50	32PIN TSOP-I
UT621024LS-70L	70	300	32PIN STSOP
UT621024LS-70LL	70	50	32PIN STSOP